CLAIMS

We claim:

1. A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

an analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits.

2. The system of Claim 1, wherein said memory receives said data at a rate of greater than 10 Mbits/sec for more than 5 seconds and stores more than 50 Mbits of said data.

3. The system of Claim 1, wherein said analog data comprises image data.

4. The system of Claim 1, wherein said image processing and compression circuits comprise an analog-to-digital (A/D) converter.

5. The system of Claim 4, wherein said image processing and compression circuits further comprise an image compressor.

6. The system of Claim 1, wherein said memory transmits portions of said data when said image processing and compression circuits are available for processing said data.

7. The system of Claim 5, wherein said image sensor, image processing and compression circuits, and memory comprise a digital still camera.

8. The system of Claim 7, wherein said memory is contained in a removable memory card.

9. The system of Claim 8, wherein said A/D converter is contained in said removable memory card.

10. The system of Claim 7, wherein said image processing and compression circuits are contained within the body of said digital still camera.

11. The system of Claim 7, wherein said image processing and compression circuits are not embedded within the body of said digital still camera.

12. The system of Claim 7, wherein said image sensor, image processing and compression circuits, and memory are contained within the body of said digital still camera.

13. The system of Claim 2, wherein said memory comprises:

a plurality of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell;

a timing circuit coupled to sequentially

start programming operations by the write circuits; and

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming operations.

14. The system of Claim 13, wherein the memory is an analog memory.

15. The system of Claim 13, wherein the write pipelines comprise:

a plurality of odd numbered pipelines; and

a plurality of even numbered pipelines, wherein

when an odd numbered pipeline and an even numbered pipeline are both performing programming operations, a selection circuit in the odd numbered pipeline selects the first voltage when the selection circuit in the even numbered pipeline selects the second voltage and a selection circuit in the odd numbered pipeline selects the second voltage when the selection circuit in the even numbered pipeline selects the first voltage.

16. The system of Claim 2, wherein said memory comprises:

a plurality of banks of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein:

during a programming cycle for a selected memory cell in the array, the

write circuit applies a first voltage to drive a current through the selected memory cell and change the threshold voltage of the selected memory cell; and

during a verify cycle for the selected memory cell, the write circuit determines whether a threshold voltage of the selected memory cell has reached a target level representing a value being written into the selected memory cell;

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming cycles; and

a timing circuit coupled to start programming cycles in the pipelines, wherein the timing circuit starts programming cycles for each bank at times that are different from when programming cycles start in the other banks.

17. The system of Claim 16, wherein the plurality of banks comprises a first bank and a second bank, and the time circuit starts programming cycles in the first bank when verify cycles start in the second bank.

18. A method for digital imaging, the method comprising:

converting an image into electrical signals;

storing said electrical signals as analog data; and

transmitting portions of said analog data for digital signal processing.

19. The method of Claim 18, further comprising pre-processing said electrical signals prior to said storing.

20. The method of Claim 18, wherein said analog data is stored at a rate greater than 10 Mbits/sec for more than 5 seconds and in a quantity greater than 50 Mbits.

21. The method of Claim 18, wherein said portions are transmitted only when said digital signal processing is available.

22. The method of Claim 18, wherein said converting and storing are performed in a digital still camera.

23. The method of Claim 18, wherein said storing comprises:

starting a first programming operation to program a first selected memory cell in a first memory array, wherein the first programming operation includes connecting a charge pump to drive a current through the first selected memory cell and change a threshold voltage in the first memory cell; and

starting a second programming operation to program a second selected memory cell in a second memory array, wherein the second programming operation includes connecting the charge pump to drive a current through the second selected memory cell and change a threshold voltage in the second memory cell, wherein starting the second programming operation occurs after starting first programming operation but before the first programming operation is complete.

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